

IN THE CLAIMS

Please cancel claims 1-30 without prejudice.

Please add new claims 31-51 as follows:

PENDING CLAIMS ARE AS FOLLOWS

1 1-30. (Cancelled)

1 31. (New) A memory control translator comprising:

2 a first bus interface for a first memory interface, the
3 first bus interface to couple to a memory control unit;

4 a second bus interface for a second memory interface,
5 the second bus interface to couple to a system memory, the
6 second memory interface differing from the first memory
7 interface;

8 a command decoder and generator coupled between the
9 first bus interface and the second bus interface, the command
10 decoder and generator to decode and translate commands for
11 the first memory interface from the memory control unit into
12 commands for the second memory interface;

13 at least one data buffer coupled between the first bus
14 interface and the second bus interface, the at least one data
15 buffer to store data;

16 at least one address buffer coupled between the first
17 bus interface and the second bus interface, the at least one
18 address buffer to store one or more addresses corresponding
19 to memory locations associated with the data stored in the at
20 least one data buffer;

21 and wherein the memory control translator to synchronize
22 commands, data and addresses between the memory control unit
23 and the system memory.

1 32. (New) The memory control translator of claim 31,
2 wherein
3 the at least one data buffer is a first FIFO buffer.

1 33. (New) The memory control translator of claim 32,
2 wherein
3 the at least one address buffer is a second FIFO buffer.

1 34. (New) The memory control translator of claim 31,
2 wherein
3 the at least one data buffer includes
4 a write data buffer for writing data into memory,
5 and
6 a read data buffer for reading data from memory.

1 35. (New) The memory control translator of claim 34,
2 wherein
3 the at least one address buffer includes
4 a column address buffer to store column addresses,
5 and
6 a row address buffer to store row addresses.

1 36. (New) The memory control translator of claim 31,
2 wherein
3 the first memory interface is an RDRAM memory interface,
4 and
5 the second memory interface is an SDRAM memory
6 interface.

1 37. (New) The memory control translator of claim 31
2 further comprising:
3 at least one address comparator to compare an address
4 from the memory control unit with an address stored in the at
5 least one address buffer, and
6 a multiplexor coupled to the at least one address
7 comparator and the at least one data buffer, the multiplexor
8 to select data from the at least one data buffer in response
9 to the at least one address comparator.

1 38. (New) The memory control translator of claim 37,
2 wherein
3 the at least one data buffer includes
4 a write data buffer for writing data into memory,
5 and
6 a read data buffer for reading data from memory,
7 and
8 the multiplexor to select data from the write data
9 buffer in response to the at least one address comparator.

1 39. (New) The memory control translator of claim 38,
2 wherein
3 the at least one address buffer includes
4 a column address buffer to store column addresses,
5 and
6 a row address buffer to store row addresses,
7 the at least one comparator includes
8 a column address comparator to compare column
9 addresses, and
10 a row address comparator to compare row
11 addresses,
12 and
13 the multiplexor to select data from the write data
14 buffer in response to the column address comparator and the
15 row address comparator.

1 40. (New) The memory control translator of claim 36,
2 wherein
3 the system memory is SDRAM memory and the memory control
4 unit generates commands for RDRAM memory.

1 41. (New) A memory control translator comprising:
2 an RDRAM memory interface to couple to a memory control
3 unit;

4 an SDRAM memory interface to couple to a system memory,
5 the SDRAM memory interface differing from the RDRAM memory
6 interface;

7 a command decoder and generator coupled between the
8 RDRAM memory interface and the SDRAM memory interface, the
9 command decoder and generator to decode and translate
10 commands received by the RDRAM memory interface from the
11 memory control unit into commands to transmit out over the
12 SDRAM memory interface to the system memory;

13 at least one data buffer coupled between the RDRAM
14 memory interface and the SDRAM memory interface, the at least
15 one data buffer to store data;

16 at least one address buffer coupled between the RDRAM
17 memory interface and the SDRAM memory interface, the at least
18 one address buffer to store one or more addresses
19 corresponding to memory locations associated with the data
20 stored in the at least one data buffer;

21 and wherein the memory control translator to synchronize
22 commands, data and addresses between the memory control unit
23 and the system memory.

1 42. (New) The memory control translator of claim 41,
2 wherein

3 the at least one data buffer is a first FIFO buffer.

1 43. (New) The memory control translator of claim 42,
2 wherein

3 the at least one address buffer is a second FIFO buffer.

1 44. (New) The memory control translator of claim 41,
2 wherein
3 the at least one data buffer includes
4 a write data buffer for writing data into memory,
5 and
6 a read data buffer for reading data from memory.

1 45. (New) The memory control translator of claim 44,
2 wherein
3 the at least one address buffer includes
4 a column address buffer to store column addresses,
5 and
6 a row address buffer to store row addresses.

1 46. (New) The memory control translator of claim 41,
2 wherein
3 the system memory is SDRAM memory and the memory control
4 unit generates commands for RDRAM memory, and
5 the command decoder and generator translates commands
6 for RDRAM memory into commands for the SDRAM memory.

1 47. (New) A memory control translator comprising:
2 an RDRAM memory interface to couple to a memory control
3 unit;

4 an SDRAM memory interface to couple to a system memory,
5 the SDRAM memory interface differing from the RDRAM memory
6 interface;

7 a command decoder and generator coupled between the
8 RDRAM memory interface and the SDRAM memory interface, the
9 command decoder and generator to decode and translate
10 commands received by the RDRAM memory interface from the
11 memory control unit into commands to transmit out over the
12 SDRAM memory interface to the system memory;

13 a write data buffer coupled between the RDRAM memory
14 interface and the SDRAM memory interface, the write data
15 buffer to store data to be written into the system memory,
16 and

17 a read data buffer coupled between the RDRAM memory
18 interface and the SDRAM memory interface, the read data
19 buffer to store data to be read from the system memory;

20 a column address buffer coupled between the RDRAM memory
21 interface and the SDRAM memory interface, the column address
22 buffer to store one or more column addresses corresponding to
23 memory locations associated with the data stored in the write
24 data buffer and the read data buffer; and

25 a row address buffer coupled between the RDRAM memory
26 interface and the SDRAM memory interface, the row address
27 buffer to store one or more row addresses corresponding to
28 the memory locations associated with the data stored in the
29 write data buffer and the read data buffer.

1 48. (New) The memory control translator of claim 47,
2 wherein

3 the memory control translator to synchronize
4 commands, data and addresses between the memory control
5 unit and the system memory.

1 49. (New) The memory control translator of claim 47,
2 wherein

3 the system memory is SDRAM memory and the memory control
4 unit generates commands for RDRAM memory, and

5 the command decoder and generator translates commands
6 for RDRAM memory into commands for the SDRAM memory.

1 50. (New) The memory control translator of claim 47,
2 wherein

3 the write data buffer is a first FIFO buffer, and

4 the read data buffer is a second FIFO buffer.

1 51. (New) The memory control translator of claim 50,
2 wherein

3 the column address buffer is a third FIFO buffer, and

4 the row address buffer is a fourth FIFO buffer.